CLAIMS

What is claimed is:

1. A method for converting a planar transistor design to a vertical double-gate transistor design, comprising:

providing a planar transistor layout corresponding to the planar transistor design having a gate layer overlying an active layer;

defining at least one intermediate layer based on an overlapping region of the gate layer and the active layer, wherein the at least one intermediate layer defines a spacing between at least two fins of the vertical double-gate transistor design; and

defining a resulting layer based on a non-overlapping region of the at least one intermediate layer and the active layer, the resulting layer for use in creating at least a portion of a mask corresponding to the vertical double-gate transistor design.

2. The method of claim 1, wherein defining at least one intermediate layer comprises:

defining a first intermediate layer based on an overlapping region of the gate layer and the active layer; and

using the first intermediate layer to define a second intermediate layer to define the spacing between the at least two fins of the vertical double-gate transistor design.

3. The method of claim 2, wherein defining the first intermediate layer based on the overlapping region of the gate layer and the active layer comprises

performing an AND function between the gate layer and the active layer to define the first intermediate layer.

4. The method of claim 2, wherein defining the resulting layer based on a non-overlapping region of the second intermediate layer and the active layer comprises performing an XOR function between the second intermediate layer and the active layer.

5. The method of claim 2, further comprising:

prior to using the first intermediate layer to define the second intermediate layer, modifying a dimension of the first intermediate layer.

6. The method of claim 5, wherein modifying the dimension of the first intermediate layer comprises increasing at least one of a length or width of the first intermediate layer by a predetermined amount.

7. The method of claim 6, wherein modifying the dimension of the first intermediate layer comprises increasing the length and the width of the first intermediate layer by the predetermined amount.

8. The method of claim 2, wherein the second intermediate layer further defines a length of the at least two fins, wherein the length is greater than a length of the gate layer in the overlapping region of the gate layer and the active layer.

9. The method of claim 8, wherein the second intermediate layer further defines a width of the at least two fins.

10. The method of claim 1, wherein the at least one intermediate layer further defines a length of the at least two fins, wherein the length is greater than a length of the gate layer in the overlapping region of the gate layer and the active layer.

11. The method of claim 10, wherein the at least one intermediate layer further defines a width of the at least two fins.

12. The method of claim 1, further comprising:

providing a semiconductor substrate; and

using the mask to create a semiconductor device overlying the semiconductor substrate, the semiconductor device comprising a vertical double-gate transistor corresponding to the vertical double-gate transistor design.

13. A method for converting a planar transistor design to a vertical double-gate transistor design, comprising:

providing a planar transistor layout corresponding to the planar transistor design having a gate layer overlying an active layer;

performing an AND function between the gate layer and active layer to define a first intermediate layer;

defining a second intermediate layer based on the first intermediate layer, the second intermediate layer defining a spacing between at least two fins of the vertical double-gate transistor design; and

performing an XOR function between the second intermediate layer and the active layer to define a resulting layer, the resulting layer for use

in creating at least a portion of a mask corresponding to the vertical double-gate transistor design.

14. The method of claim 13, further comprising:

providing a semiconductor substrate; and

using the mask to create a semiconductor device overlying the semiconductor substrate, the semiconductor device comprising a vertical double-gate transistor corresponding to the vertical double-gate transistor design.

15. The method of claim 13, further comprising:

prior to using the first intermediate layer to define the second intermediate layer, performing an oversize function on the first intermediate layer.

16. The method of claim 15, wherein performing the oversize function comprises increasing at least one of a length or width of the first intermediate layer by a predetermined amount.

17. The method of claim 13, wherein the second intermediate layer further defines a length of the at least two fins, wherein the length is greater than a length of the gate layer in the overlapping region of the gate layer and the active layer.

18. The method of claim 17, wherein the second intermediate layer further defines a width of the at least two fins.

19. A method for converting a planar transistor design to a vertical double-gate transistor design stored via a computer readable medium, said computer readable medium comprising:

a first set of instructions for receiving a planar transistor layout corresponding to the planar transistor design having a gate layer overlying an active layer;

a second set of instructions for defining at least one intermediate layer based on an overlapping region of the gate layer and the active layer, wherein the at least one intermediate layer defines a spacing between at least two fins of the vertical double-gate transistor design; and

a third set of instructions for defining a resulting layer based on a non-overlapping region of the at least one intermediate layer and the active layer, the resulting layer for use in creating at least a portion of a mask corresponding to the vertical double-gate transistor design.

20. The computer readable medium of claim 19, wherein the second set of instructions comprises:

a fourth set of instructions for defining a first intermediate layer based on an overlapping region of the gate layer and the active layer; and

a fifth set of instruction for using the first intermediate layer to define a second intermediate layer to define the spacing between the at least two fins of the vertical double-gate transistor design.